

WHAT IS CLAIMED IS:

- 1 1. A memory shared by a plurality of heterogeneous
2 processors, comprising:
3 the shared memory;
4 wherein the shared memory is accessible by one or more
5 first processors that are adapted to process a first
6 instruction set; and
7 wherein the shared memory is accessible by one or more
8 second processors that are adapted to process a second
9 instruction set.
- 1 2. The shared memory as described in claim 1 further
2 comprising:
3 a memory map corresponding to the shared memory,
4 wherein the memory map is shared between the first
5 processors and the second processors.
- 1 3. The shared memory as described in claim 2 further
2 comprising:
3 an operating system that operates on one of the first
4 processors, the first processor controlling the memory
5 map.
- 1 4. The shared memory as described in claim 1 wherein each
2 second processor further comprises:
3 a synergistic processing unit;
4 a local storage; and
5 a memory management unit, the memory management unit
6 including a direct memory access controller.

1 5. The shared memory as described in claim 4 wherein at
2 least one of the second processors use the direct
3 memory access controller to access the shared memory.

1 6. The shared memory as described in claim 4 wherein the
2 local storage is divided into a private storage and a
3 non-private storage.

1 7. The shared memory as described in claim 6 wherein the
2 non-private storage is included in the shared memory.

1 8. The shared memory as described on claim 1 wherein the
2 memory map includes a plurality of regions, wherein at
3 least one of the regions is selected from the group
4 consisting of an external system memory region, a
5 local storage aliases region, a TLB region, an MFC
6 region, an operating system region, and an I/O devices
7 region.

1 9. The shared memory as described in claim 1 wherein the
2 memory, the first processors, and the second
3 processors are included on one substrate.

1 10. The shared memory as described in claim 1 wherein the
2 shared memory, the first processors, and the second
3 processors are connected using an on chip coherent
4 multi-processor bus.

1 11. A method for sharing a memory between a plurality of
2 heterogeneous processors, said method comprising:
3 receiving a memory request;
4 allocating a first memory partition on the shared
5 memory that corresponds to the memory request, the

first memory partition accessible by one or more first processors that are adapted to process a first instruction set; and

assigning a second memory partition on the shared memory to one or more second processors that are adapted to process a second instruction set.

12. The method as described in claim 11 further comprising:
managing the first memory partition and the second memory partition using a common memory map.

13. The method as described in claim 12 wherein one of the first processors includes an operating system whereby the first processor controls the common memory map.

14. The method as described in claim 12 wherein the common memory map includes a plurality of regions, wherein at least one of the regions is selected from the group consisting of an external system memory region, a local storage aliases region, a TLB region, an MFC region, an operating system region, and an I/O devices region.

15. The method as described in claim 11 wherein at least one of the first processors is a Power PC and wherein at least one of the second processors is included in a synergistic processing unit.

16. The method as described in claim 15 wherein the shared memory corresponds to the synergistic processing unit.

1 17. The method as described in claim 11 wherein at least
2 one of the second processors uses a direct memory
3 access controller for accessing the shared memory.

4 18. A computer program product stored on a computer
5 operable media for sharing a memory between a
6 plurality of heterogeneous processors, said computer
7 program product comprising:
8 means for allocating a first memory partition on the
9 shared memory that corresponds to the memory request,
10 the first memory partition accessible by one or more
11 first processors that are adapted to process a first
12 instruction set; and
13 means for assigning a second memory partition on the
14 shared memory to one or more second processors that
15 are adapted to process a second instruction set.

1 19. The computer program product as described in claim 18
2 further comprising:
3 means for managing the first memory partition and the
4 second memory partition using a common memory map.

1 20. The computer program product as described in claim 19
2 wherein one of the first processors includes an
3 operating system whereby the first processor controls
4 the common memory map.

1 21. The computer program product as described in claim 19
2 wherein the common memory map includes a plurality of
3 regions, wherein at least one of the regions is
4 selected from the group consisting of an external

5 system memory region, a local storage aliases region,
6 a TLB region, an MFC region, an operating system
7 region, and an I/O devices region.

1 22. The computer program product as described in claim 18
2 wherein at least one of the first processors is a
3 Power PC and wherein at least one of the second
4 processors is included in a synergistic processing
5 unit.

1 23. The computer program product as described in claim 22
2 wherein the shared memory corresponds to the
3 synergistic processing unit.

1 24. The computer program product as described in claim 18
2 wherein at least one of the second processors uses a
3 direct memory access controller for accessing the
4 shared memory.

1 25. A memory shared by a plurality of heterogeneous
2 processors, comprising:
3 the memory, wherein the memory includes one or more
4 non-private storage areas, the non-private storage
5 areas corresponding to one or more second processors
6 that are adapted to process a second instruction set
7 and access the memory; and
8 wherein the shared memory is accessible by one or more
9 first processors that are adapted to process a first
10 instruction set and access the memory.

1 26. The shared memory as described in claim 25 wherein
2 each second processor further comprises:

3 synergistic processing logic which uses private
4 storage, the private storage not included in the
5 shared memory; and
6 memory management logic for directly accessing the
7 shared memory.

1 27. The shared memory as described in claim 25 further
2 comprising:
3 memory mapping logic that corresponds to the shared
4 memory, wherein the memory mapping logic is shared
5 between the first processors and the second
6 processors.

1 28. The shared memory as described in claim 27 further
2 comprising:
3 an operating system that operates on one of the first
4 processors, the first processor controlling the memory
5 mapping logic.

1 29. The shared memory as described in claim 25 wherein one
2 of the first processors configures each of the non-
3 private storage areas.